BUILD A HIGH PERFORMANCE THD ANALYZER

PART TWO

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Last month we discussed the theory of operation of total harmonic distortion (THD) analyzers, the features of the analyzer being described here, many of the underlying principles, and finally the details of the signal source portion of the analyzer. This month we will resume the circuit description by starting with the input circuits and the state-variable bandpass filter. Before we go into the remainder of the analyzer, let me present the printed wiring board layout for the signal source, CP1, as Fig. 10 and the corresponding component placement as Fig. 11. I also repeat Fig. 5, which is the block diagram of the analyzer, for clarity.

Input Circuit and Bandpass Filter

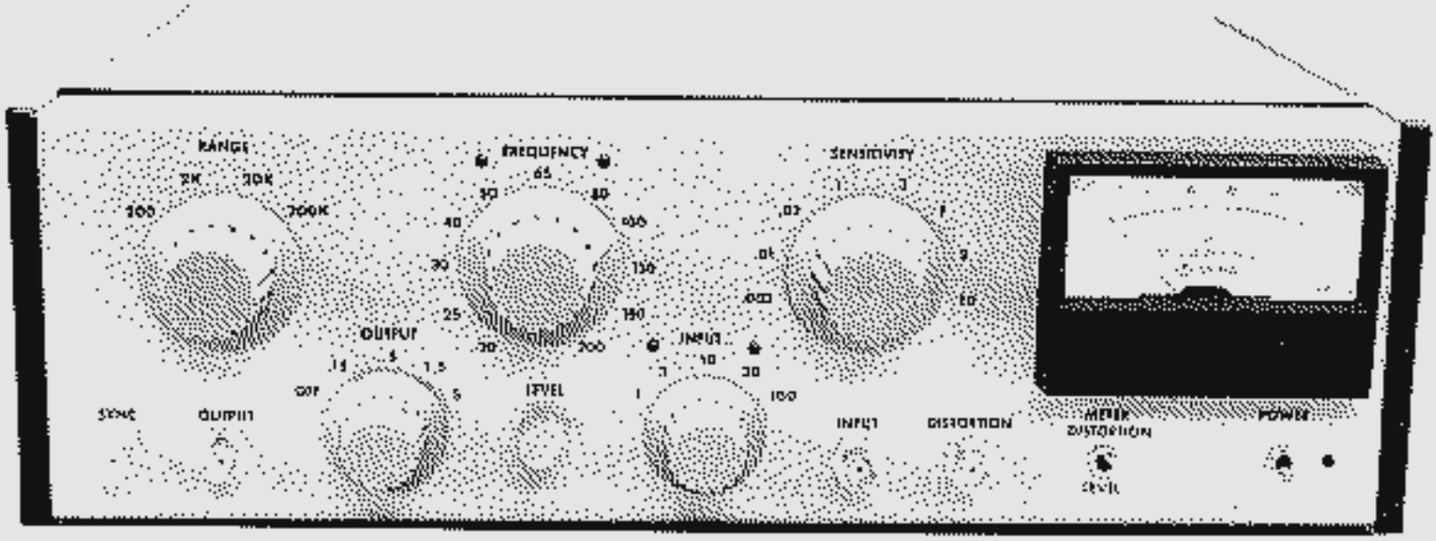
The input attenuator, input amplifier, and voltage-controlled state-variable bandpass filter are shown in Fig. 12.

The input attenuator (S4) selects an appropriate input sensitivity for maximum operating levels of 100 V, 30 V, 10 V, 3 V, or 1 V. The "nominal" operating levels are a third of these values. Because of the auto-set level feature, actual input levels which are above or below the nominal level by as much as 10 dB can be accommodated; no input vernier control is required. Notice that on the 1-V range a gain-of-three amplifier (IC9) is switched into the circuit to boost a nominal 0.33-V signal to the nominal 1-V internal analyzer operating level. The input impedance of the analyzer is 100 kilohms on all input ranges.

Because of the high impedances in the attenuator circuit, S4 and its associated components must be placed in a small shielded enclosure in order to avoid stray pickup and oscillations. Depending on stray switch capacitances, small capacitors, such as those shown dotted in Fig. 12, may have to be added to obtain a flat frequency response at all attenuator settings.

The heart of the signal processing in the analyzer is the voltage-controlled state-variable bandpass filter. Its primary function is to deliver a fundamental signal to the differential amplifier (not shown in Fig. 12) whose amplitude and phase are such that the fundamental will be exactly cancelled, leaving only distortion products. In addition, very little of the signal's distortion products should be passed by the bandpass filter so that little or no cancellation or attenuation of distortion products will occur at the differential amplifier. As mentioned earlier, in order to achieve exact fundamental nulling, the gain and center frequency of the bandpass filter are precisely controlled by the auto-tune circuits (Fig. 5).

The state-variable filter in Fig. 12 is a bit more complicated than the simple one illustrated last issue in Fig. 8, but the operating principle is exactly the same. It consists of ICs 10 to 13 and 15. The use of two extra inverters in the loop



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(IC11, 13) accounts for the additional ICs. The extra inverter at IC11 permits the bandwidth-setting feedback path (R57 and R62) to be connected in such a way that center frequency changes do not affect filter Q or gain. This type of connection was also used in the oscillator, but there the extra inverter was not needed because of the sign flexibility afforded by the multiplier.

The second inverter (IC13) is required to re-establish the correct polarity for the main feedback loop (R58 and R59) and also provides a useful summing point for the amplitude and frequency control signals from the multipliers. In further contrast to the simple state-variable filter, the input signal is here applied to the noninverting input of IC10. This yields a slight noise advantage and also provides the correct signal polarity at the output of the bandpass filter. Because the bandpass filter has a gain of about 5 at the center frequency, some attenuation of the input signal is necessary (R54 and R55) to establish the proper operating level at its output. The center frequency and gain of the filter are trimmed by R59 and R62 respectively.

Control of the center frequency of the bandpass filter is quite simple. Recall from our earlier discussion that the center frequency of a state-variable bandpass filter can be changed by simply adjusting the loop gain. In Fig. 12 this is accomplished by connecting a multiplier and series resistor (R65) around the inverter formed by IC13 to provide controlled amounts of negative or positive feedback. When the multiplier provides a noninverted characteristic, additional negative feedback is provided around the inverter, making its gain less than unity and consequently lowering the center frequency of the filter. The opposite action results when the multiplier provides an inverted characteristic. In this manner the gain of the inverter can be controlled over a ±3.2 percent range, resulting in a center frequency control range of ±1.6 percent.

The multiplier consists of FET Q5 and IC14, and it is identical to the one used in the oscillator (Fig. 9, Part I). As in the oscillator, any distortion introduced by the control circuit must pass through two integrators before reaching the output (E18), and is thus substantially reduced.

Amplitude control of the bandpass filter is a bit more subtle. Based on last month's discussion of the simple state-variable filter, one's first inclination is to change the gain of the filter by changing the amount of the "damping" feedback, here provided by R57 and R62. This will surely accomplish the desired control, but notice that in this case any distortion injected by the control circuit will be removed from the filter output by only one integrator. To minimize distortion, we would like to inject the amplitude control signal at the same advantageous point as the frequency control signal, i.e., at the input of inverter IC13. Fortunately, it turns out that a small amount of feedback (positive or negative) around the *second* integrator (IC15) is equally effective in providing control of the gain as

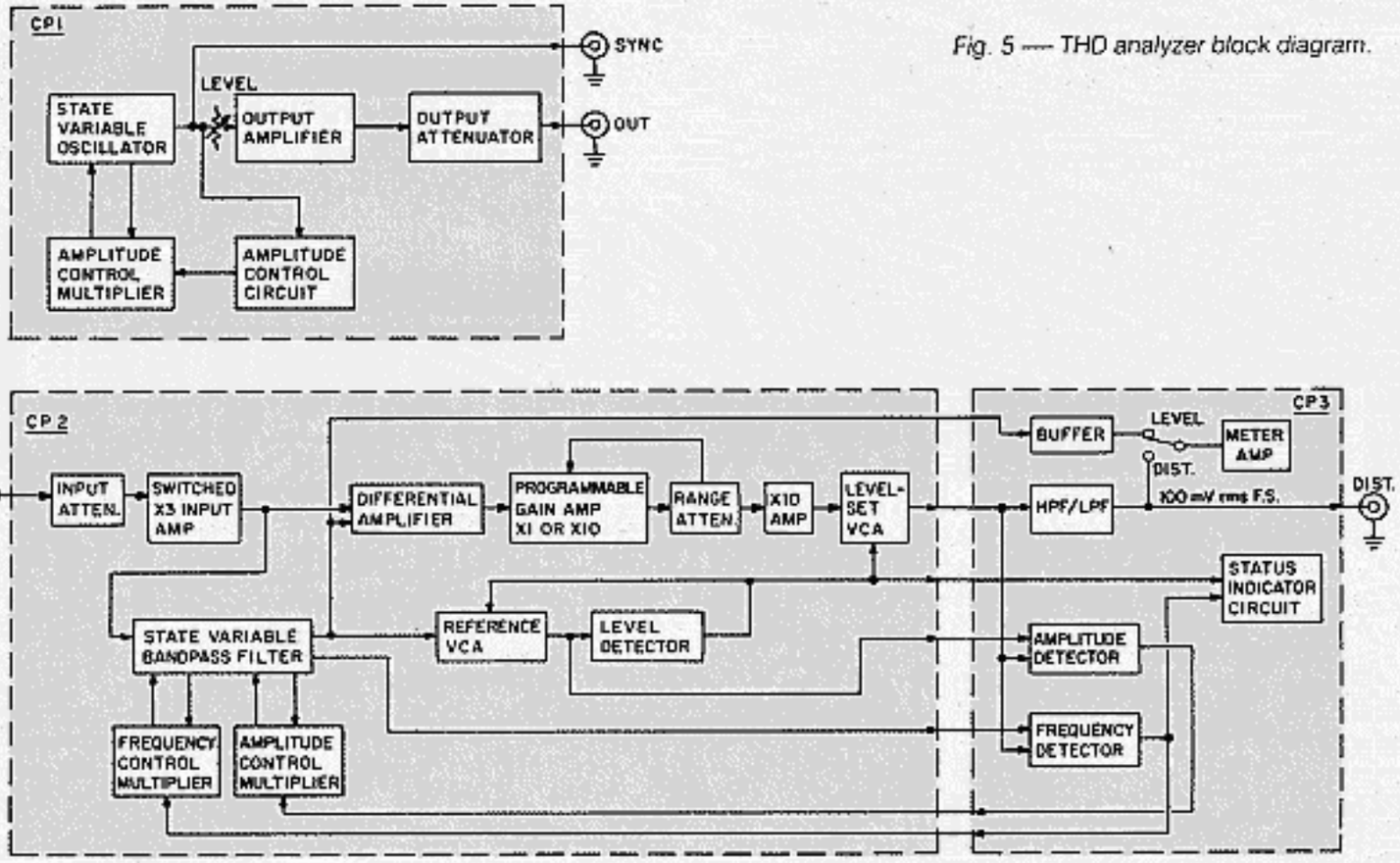

Fig. 5 — THD analyzer block diagram.

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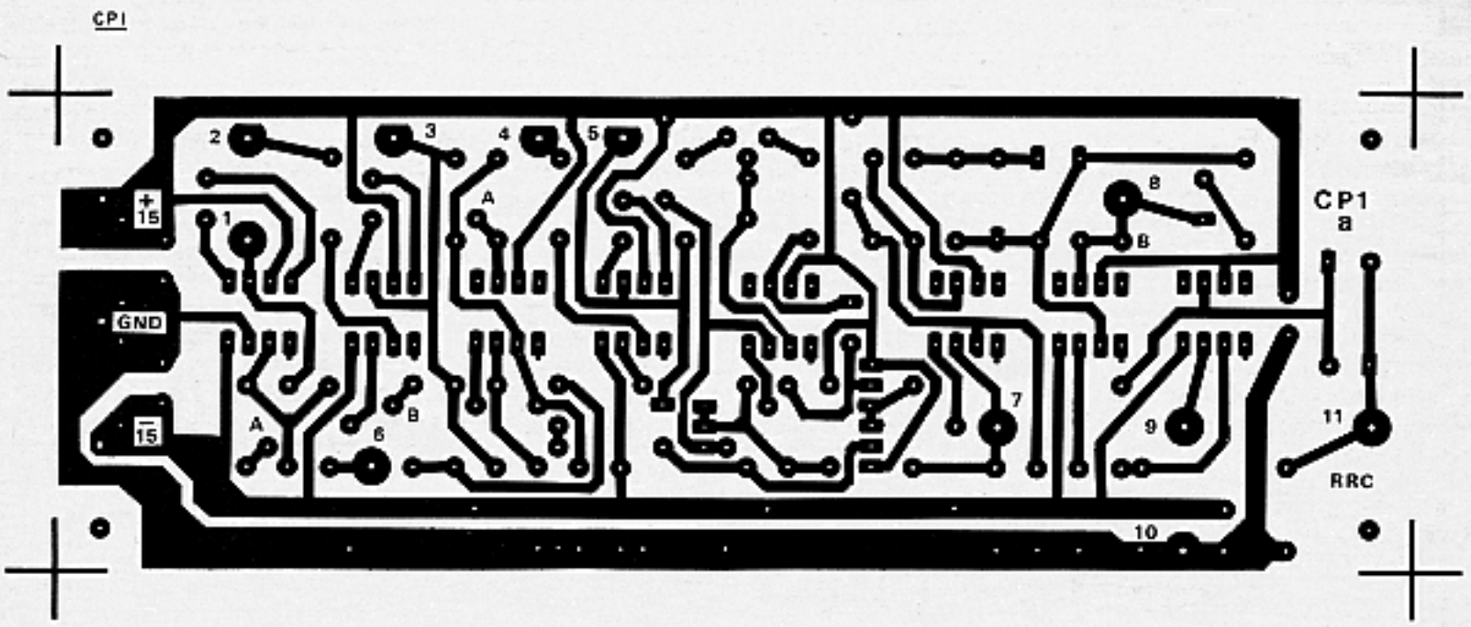

Fig. 10 — Printed wiring board layout for CP1, the signal source.

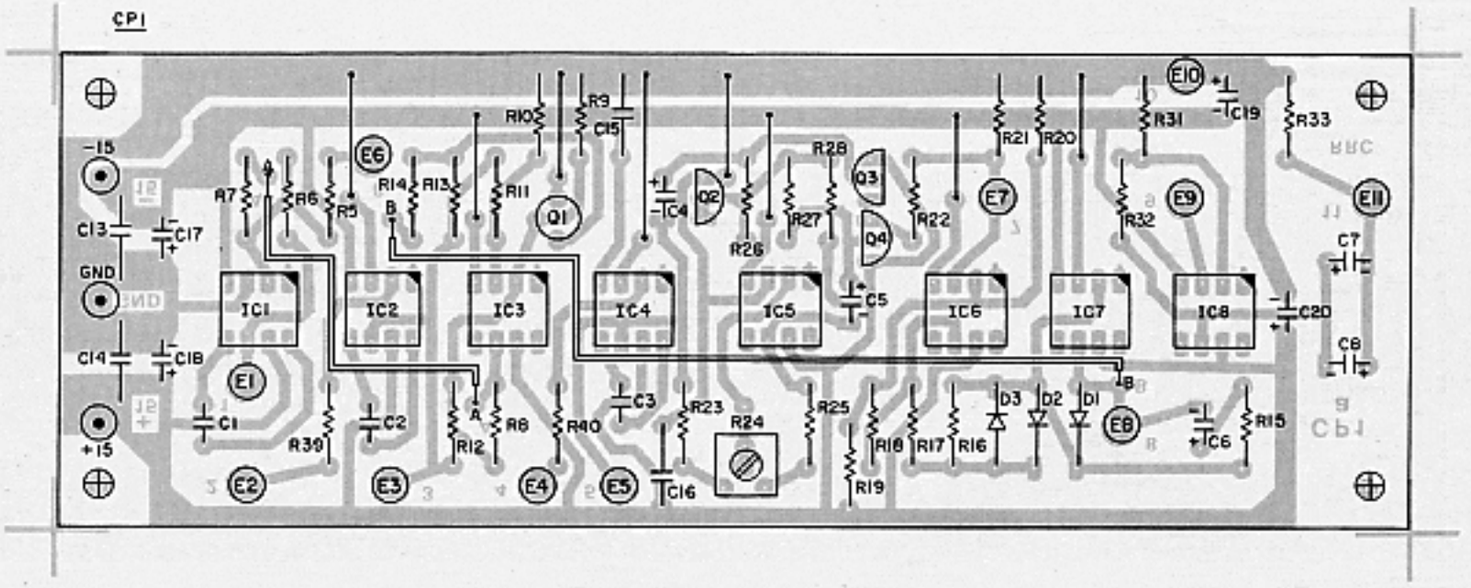

Fig. 11 — Parts placement for CP1, the signal source.

long as the perturbation is small, as it is here. The amplitude control multiplier, consisting of FET Q6 and IC16, thus provides amplitude control feedback from the output of IC15 to the input of inverter IC13. An amplitude control range of about ±3.5 percent results.

Differential and Product Amplifiers

The differential amplifier which completes the notch filter and the distortion product amplifiers are shown in Fig. 13. Also shown here is the auto-set level circuit which will be discussed shortly.

IC17 functions as the differential amplifier where the fundamental supplied by the bandpass filter is subtracted from the input signal. The combination of this differential amplifier and the bandpass filter thus comprises the notch filter. The differential amplifier also provides a gain of 10 to the distortion products. The input signal (E15) is applied directly to the high-impedance noninverting input of IC17 while the fundamental from the bandpass filter (E18) is applied to the inverting input through R84. Because of the attenuation which results from the voltage divider formed by R84 and R85, nulling results when the fundamental from the bandpass filter is about 10 percent larger than the fundamental sup-

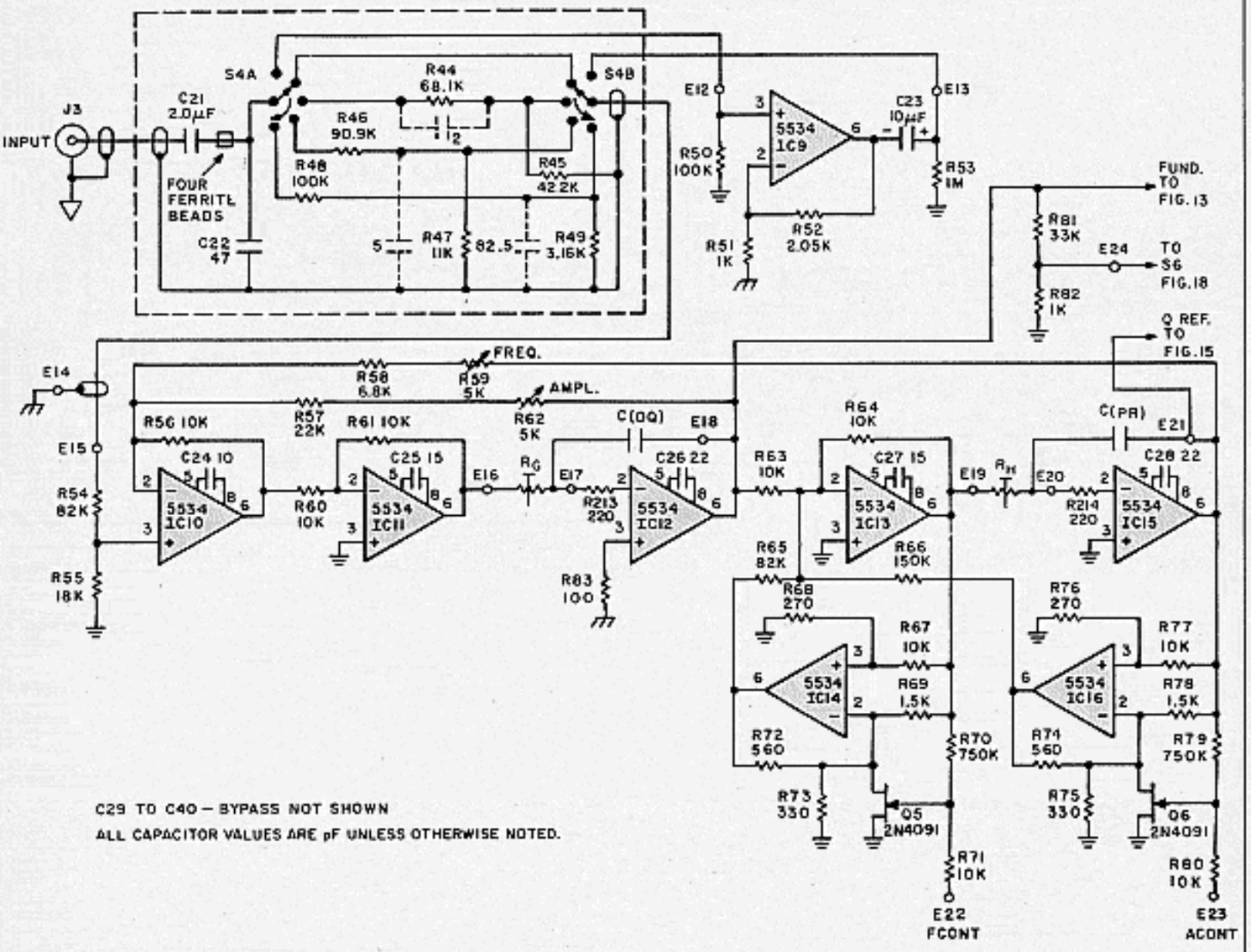

Fig. 12 — THD analyzer voltage-controlled bandpass filter.

plied directly from the input attenuator.

The differential amplifier is followed by another amplifier (IC18) whose gain is 10 on all distortion ranges except the 10 percent and 3 percent full-scale ranges, where it is unity. The gain of this stage is switched by a FET whose gate voltage is controlled by the sensitivity switch (S5). IC18 is followed by an attenuator which is also controlled by S5, establishing full-scale sensitivities of 10, 3, 1, 0.3, 0.1, 0.03, 0.01, and 0.003 percent. This is followed by a fixed gain-of-ten amplifier (IC19). The distortion product signal then proceeds to the auto-set level voltage-controlled amplifier (ICs 20 & 21).

Voltage-Controlled Amplifiers

Because the voltage-controlled amplifiers (VCA) are central to the operation of the auto-set level circuitry, we will discuss their operation before proceeding further.

A simple VCA is shown in Fig. 14. It consists of a 1496-type balanced modulator IC (whose internal circuit is shown) and an op-amp.

The op-amp is connected as an inverting feedback amplifier, the ratio of whose input and feedback signals is controlled by the 1496. As this ratio is varied from a very small number, through unity and on to a very large number, the gain changes proportionately from small to large. In fact, in this circuit the gain is numerically equal to the ratio. A d.c. control voltage applied to the 1496 controls this ratio and thus the gain.

Referring to Fig. 14, bias resistor R3 sets up a bias current in Q7 and Q8 of about 1 mA. Transistors Q5 and Q6 are connected as common-base stages and provide a low-impedance point at their emitters where a.c. signal currents can

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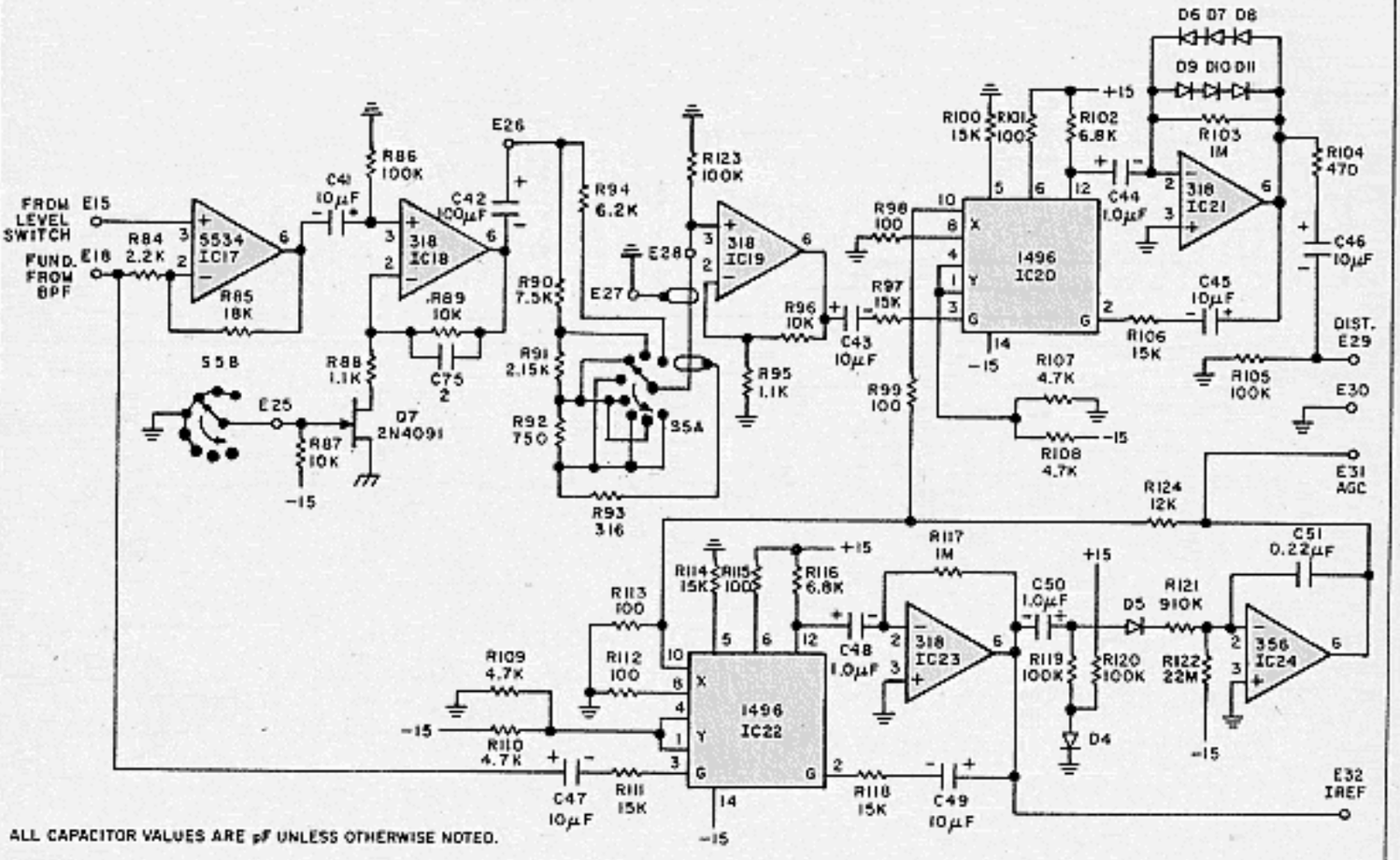

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Fig. 13 — THD analyzer product amplifier and level set.

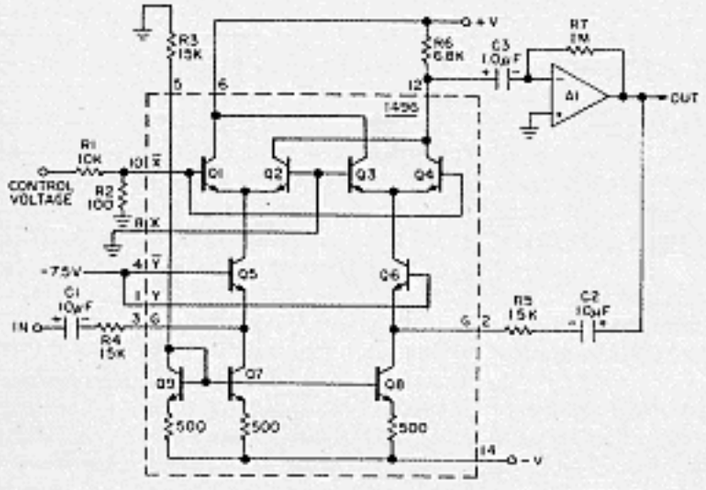

Fig. 14 — A simple voltage-controlled amplifier (VCA).

be added to the d.c. bias currents. The input signal current established by R4 is applied to the emitter of Q5, while the feedback current established by R5 is applied to the emitter of Q6. The action in the upper "quad" of transistors (Q1-Q4) determines what portion of each of these a.c. signals reaches the output at pin 12 and thus the inverting input of the operational amplifier.

We see that at the collector of Q5 we have d.c. bias current plus a.c. input signal, while at the collector of Q6 we have d.c. bias current plus a.c. feedback signal. Each of these currents is applied to the emitters of a differential pair, where some will flow in one emitter and the remainder will flow in the other emitter of a

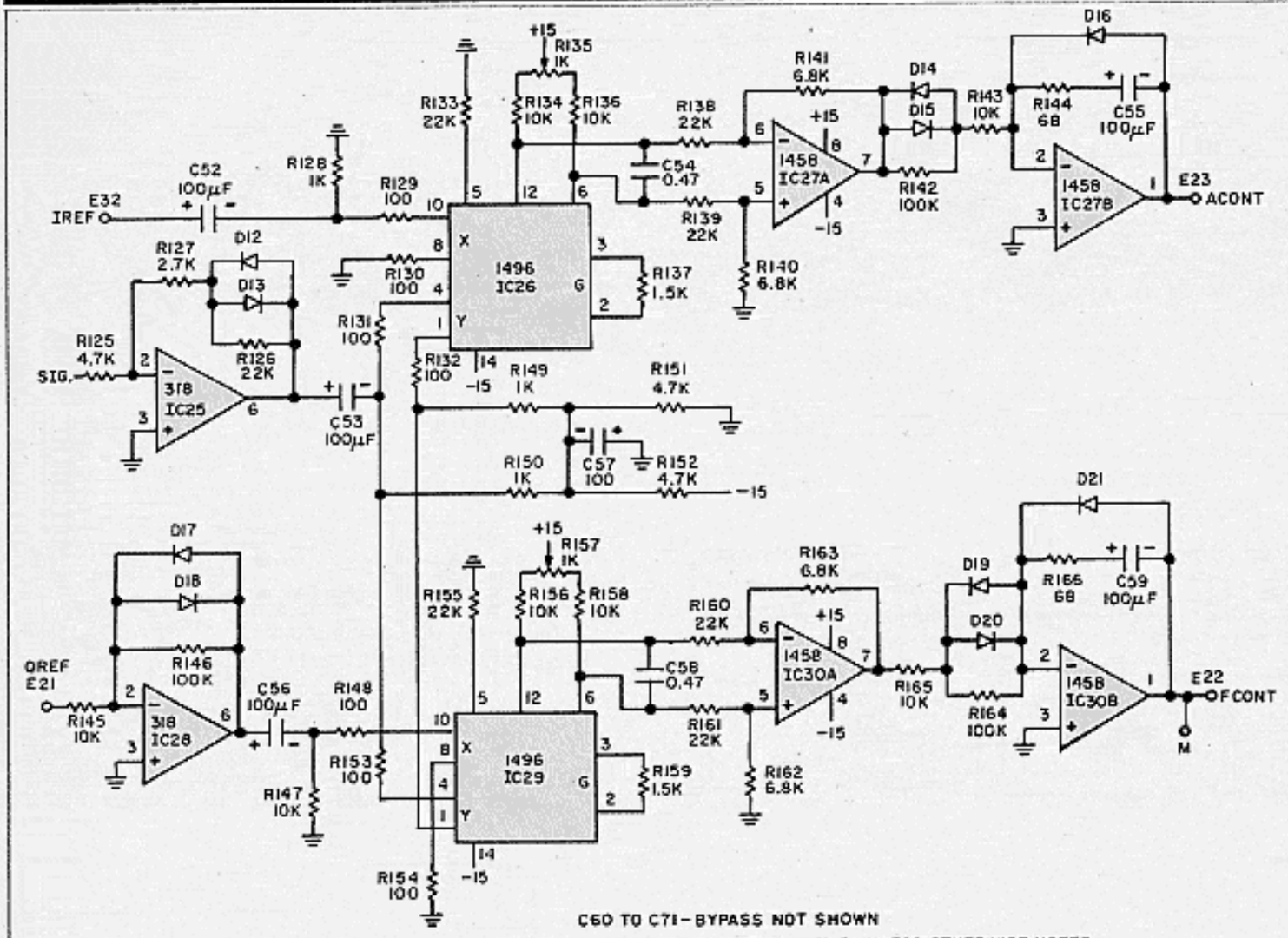

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Fig. 15 — THD analyzer amplitude and frequency detectors.

given pair. Each of these currents thus splits in some proportion. The key operating principle in this circuit is that the a.c. currents into the emitters of a differential pair will split in the same proportion as the d.c. bias currents flowing into the pair.

The attenuated control voltage applied to pin 10 controls this split. When the control voltage is zero, both transistors in each differential pair have the same base voltage and conduct equally. In this case, half of the input signal and half of the feedback signal current reach the output at pin 12 via Q2 and Q4 respectively. Because of the extremely high gain of A1, the signal and feedback currents at pin 12 must essentially can-

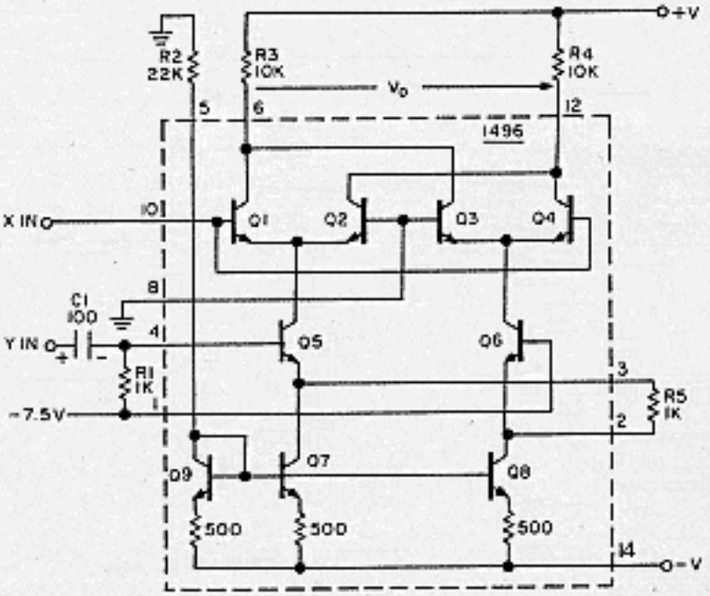

Fig. 16 — A simple phase detector.

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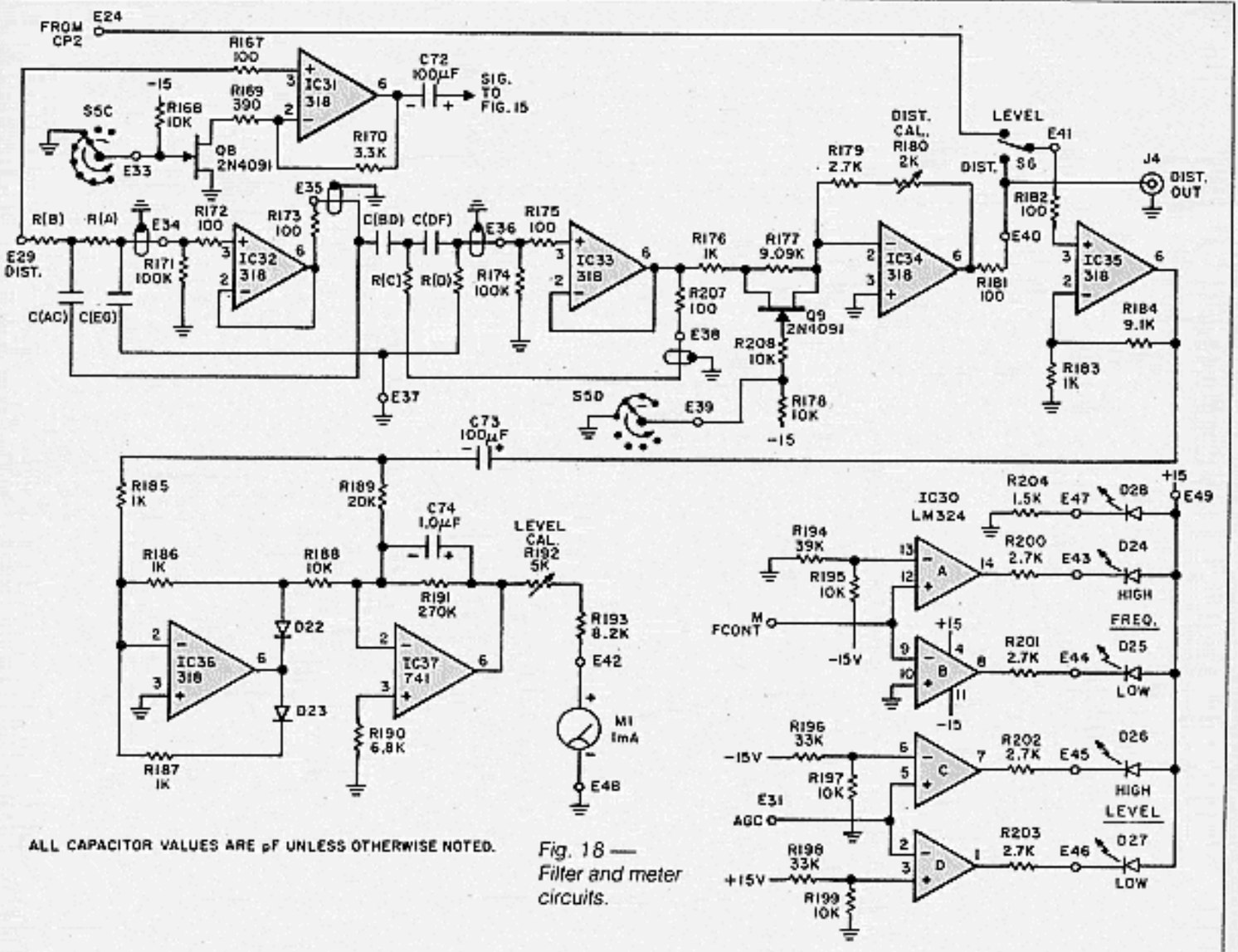

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Fig. 18 — Filter and meter circuits.

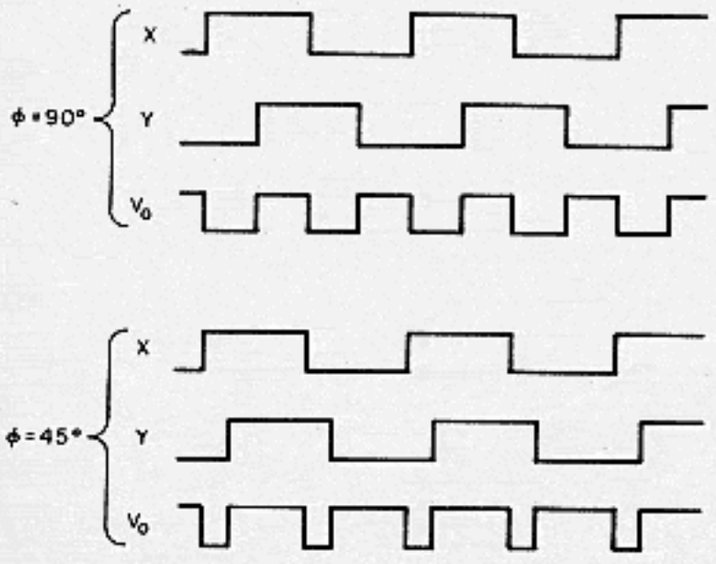

Fig. 17 — Phase comparator operation.

cel each other for finite output levels from A1. They must therefore be virtually equal. This in turn indicates that the signal currents in R4 and R5 must be equal for a zero control voltage, implying unity gain.

A positive control voltage at pin 10 will cause Q1 and Q4 to conduct more heavily than Q2 and Q3. Thus, a greater proportion of feedback current reaches pin 12 (via Q4) than input current (via Q2). In order to maintain cancellation of the two currents at pin 12, the input signal must be larger to begin with than the feedback current, implying less than unity gain. As an example, it is well known that a potential of about 60 mV across

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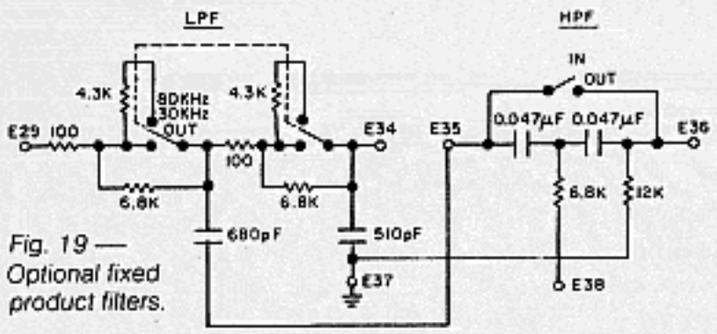

Fig. 19 — Optional fixed product filters.

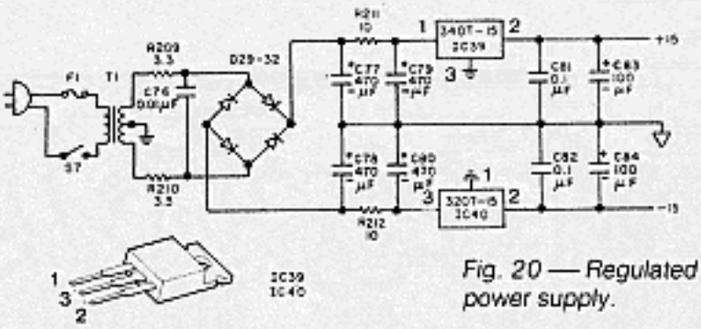

Fig. 20 — Regulated power supply.

the bases of a differential pair will cause a 10-to-1 ratio of conduction in the two transistors. In this application, a +60 mV control voltage at pin 10 will thus result in a gain of about 0.1. The situation is the inverse for a negative control voltage; a -60 mV level at pin 10 will result in a gain of about 10.

A particularly nice feature of this arrangement is that the gain in decibels is a linear function of the control voltage. Here we get a variation of 20 dB/60 mV or about 0.33 dB per mV. The 100-to-1 attenuator formed by R1 and R2 simply allows for more manageable control voltages (3.3 dB per volt). The gain control range here is in excess of ±20 dB.

Auto-Set Level Circuit

With a knowledge of the operation of the VCA, the auto-set level circuit in Fig. 13 becomes easy to understand. It consists of two identical VCAs, each with the same control voltage and thus each with the same gain. The first VCA (IC20, 21) controls the gain in the distortion product signal path and receives its input from IC19. It produces the level-adjusted distortion product output at E29 for use on CP3. The second ("reference") VCA (IC22, 23) controls the gain in an automatic gain control (a.g.c.) loop; its input is the filtered fundamental output from the bandpass filter (E18).

In addition to the reference VCA, the a.g.c. loop includes a level detector (D5) and an op-amp (IC24) connected as an integrator. The d.c. output of the integrator is the control voltage for the VCAs. The a.g.c. circuit is arranged so that the integrator will always adjust the gain of the reference VCA so that the level of the fundamental at its output is 1.1 V rms. Thus, if the input to the notch filter is the nominal 1-V level, the fundamental from the bandpass filter will be 1.1 V and the gain of both VCAs will be unity, as it should be for this situation. If the input signal level were to increase to 2 V, the gain of both VCAs would drop to 0.5, implementing the proper gain correction in the distortion product signal path.

Auto-Tune Control Circuits

The amplitude and frequency detectors which comprise the auto-tune control circuit are shown in Fig. 15. If the gain and center frequency of the bandpass filter are not perfect, the notch filter will not produce a complete null of the fundamental signal. Some fundamental will thus appear in the distortion-product signal path. An amplitude error will produce a "left-over" fundamental component whose phase is zero (or 180) degrees relative to the input signal. A fundamental component with this phase relationship is said to be a "normal" component. A frequency error will produce a so-called "quadrature" fundamental component whose phase is either leading or lagging 90 degrees relative to the input signal.

The amplitude detector functions by looking for normal fundamental components in the distortion signal and adjusting the bandpass filter gain up or down depending on the phase relationship (0 or 180 degrees). It ignores quadrature fundamental components. Similarly, the frequency detector functions by looking for quadrature fundamental components and adjusting the filter center frequency up or down depending on the phase relationship (lagging or leading). It ignores normal fundamental components.

The special detector circuit which possesses the properties mentioned above is called a "phase detector" because it is sensitive to the phase of the signal being detected. An ordinary envelope detector or rectifier is not suitable because it will detect the signal regardless of its phase. Here, the phase of the "left-over" fundamental is a crucial piece of information.

A simplified schematic of a phase detector is shown in Fig. 16. Like the VCA, it is based on the 1496-type balanced modulator IC. The phase detector is a more conventional use of this IC. Bias resistor R2 sets up an appropriate current flow in current sources Q7 and Q8. The application of a positive input signal at the Y input will cause Q5 to conduct more current than Q6; the opposite will occur for a negative input signal. A positive input at the X input will cause Q1 and Q4 to be "on" and Q2 and Q3 to be "off." The output (V_o) is taken differentially between pins 6 and 12.

We can easily see what polarity of output will be produced for any combination of positive or negative X and Y inputs. For example, if X and Y are both positive, most of the current flow is in Q5 and Q1, pulling pin 6 lower than pin 12 and producing a positive output. In general, a positive output is produced when both inputs have a like sign, and a negative output is produced when the X and Y inputs have differing signs. In a sense, this circuit performs similarly to the "EXCLUSIVE NOR" logic function. We immediately see that two perfectly in-phase signals at X and Y will always have the same sign and thus produce a maximum positive output.

The diagram in Fig. 17 lends further insight into the phase sensitivity of this type of detector. Square-wave inputs are shown for simplicity of illustration, but the circuit functions similarly for other waveforms. In the top illustration we see what happens when the X and Y inputs are 90 degrees out of phase; the average d.c. output at V_o (which is what matters) is zero. This illustrates how the amplitude detector can ignore a quadrature component.

It is easy to see that if we slide the Y

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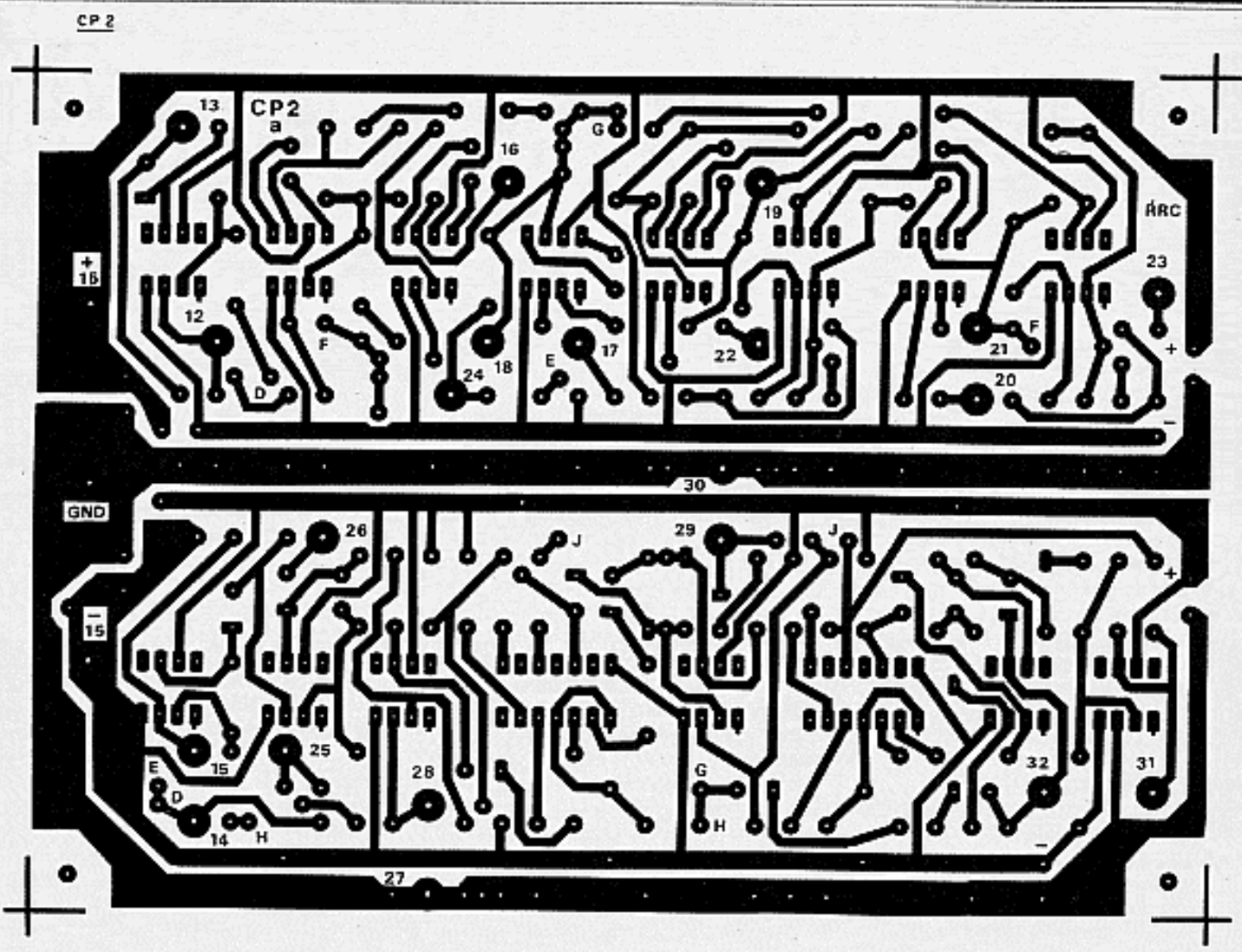

Fig. 21 — Printed circuit board CP2 for the input circuit, bandpass filter, product amplifiers, and auto-set level circuits.

input back and forth along the time axis, an asymmetry will be produced in the V_o waveform, corresponding to an average d.c. value.

The bottom illustration depicts a 45-degree relationship between the X and Y inputs. By trigonometry we can argue that the Y signal consists of equal portions of normal and quadrature components in this case. This would be representative of a situation where there were both amplitude and frequency errors simultaneously. We see that in this case a positive average d.c. output is produced at V_o. It is not, of course, quite as strongly positive as when X and Y are perfectly in phase.

We can see that if we apply an "unknown" signal to the Y input and a "reference" signal to the X input, the detector will respond to components in the unknown signal whose phase is similar to (or the inverse of) that of the reference. Components in quadrature with the reference will be ignored. In addition, the effects of noise and signals at other frequencies will average out to zero.

Returning to Fig. 15, the amplitude detector consists of ICs 25-27. The distortion product signal ("unknown") is taken from the output of IC31 (Fig. 18) and passes through IC25 where it sees a small-signal gain of five and is soft-limited beginning at ±0.7 V swings by the feedback diodes. The signal is then applied to the Y input of IC26 where it is phase-compared with a "normal" fundamental provided by the output of the reference VCA (IC23).

The differential output of the phase detector is filtered and applied to IC27A where it is converted to a single-ended signal. This signal drives the integrator (IC27B) to produce the appropriate gate voltage for the amplitude control FET (Q6). The integrator will continue to adjust the gate voltage until the output of IC27A is driven to zero. Notice that when the error from IC27A is greater than ±0.7 V, D14 and D15 conduct and speed up the integrator to achieve

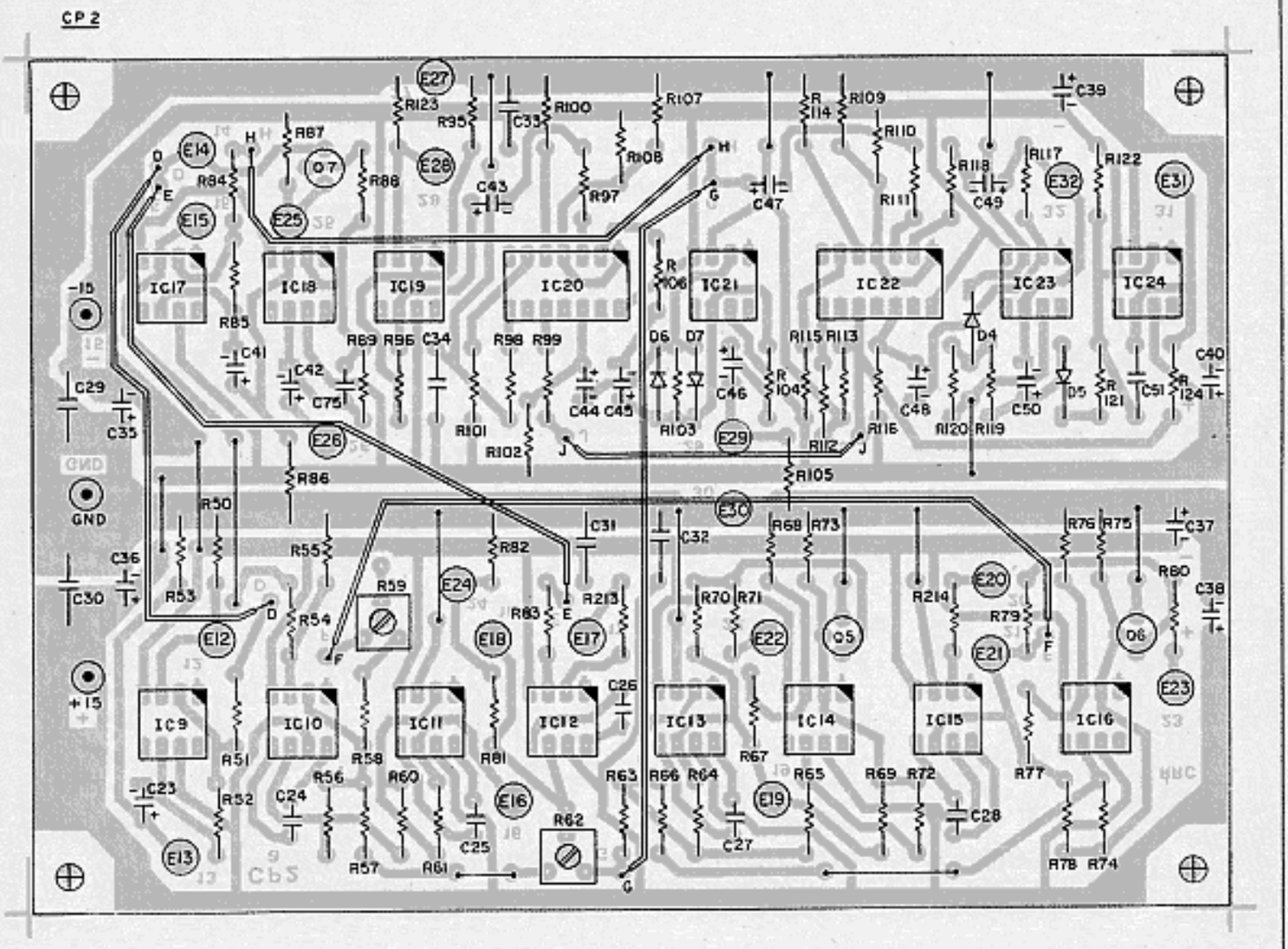

Fig. 22 — Component placement for CP2.

faster tuning following a transient.

Operation of the frequency detector (ICs 28-30) is identical to that of the amplitude detector except that it is supplied with a quadrature fundamental reference (lagging 90 degrees) instead of a normal fundamental reference. The quadrature reference is supplied from the low-pass output (IC15) of the state-variable filter and passed through amplifier-limiter IC28 before application to the X input of IC29.

Filter and Meter Circuits

The filtering, metering, and status indicator circuits are shown in Fig. 18. The distortion product signal from the auto-set level VCA on CP2 (E29) is first amplified by a factor of one or 10 in IC31 to keep it at a reasonable level for use by the auto-tune circuits for all sensitivity settings of S5. Switch S5C sets the gain of this stage to 10 on the 0.03- through 10-percent sensitivity ranges to compensate for attenuation introduced by the S5A attenuator on these ranges. Note that S5C does not affect gain in the distortion metering path.

The distortion product signal from E29 is also applied to the low-pass product filter. As mentioned earlier, the second-order Bessel low-pass product filter is set for a 3-dB cutoff frequency equal to 10 times the fundamental frequency. The filter consists of a pair of resistors (on S3), a pair of capacitors (on S1) and an op-amp (IC32) connected as a voltage follower [3]. This filter is followed by the second-order high-pass filter (IC33) which is similarly realized. Its filter Q is chosen to provide a slight gain bump at the second harmonic frequency to partly offset the small loss in the notch filter at this frequency. For reasons of high-frequency filter stability, the high-pass filter has the same set of cutoff frequencies on the 200-kHz range as on the 20-kHz range.

As mentioned in Part I, the tracking product filters add a considerable portion of the switching complexity and ex-

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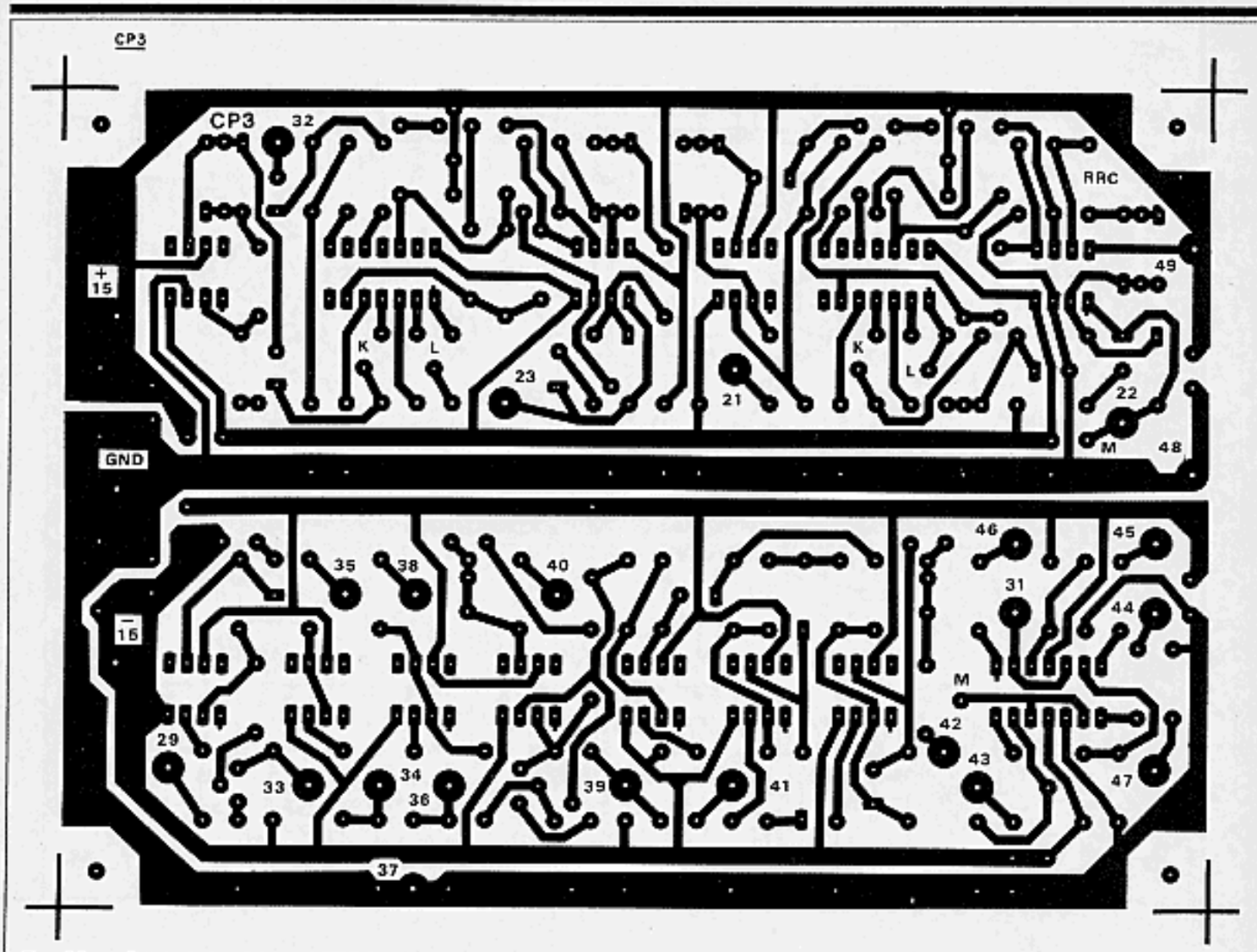

Fig. 23 — Printed circuit board CP3 for the auto tune control, product filter, meter and status indicator circuits.

pense (about $25.00) to the analyzer. Many professional analyzers provide only a switchable 400-Hz high-pass filter and a low-pass filter which can be set to 30 or 80 kHz or switched out. This simpler filtering approach can be implemented as shown in Fig. 19 with a SPST switch for the high-pass and a center-off DPDT switch for the low-pass. Use of this simpler filtering will typically result in an increase of the analyzer's residual by 0 to 3 dB and will make the reading somewhat more susceptible to hum and noise in the UUT.

Following the filters, the distortion product signal is brought to a 100-mV full-scale level by the switched-gain amplifier composed of FET Q9 and IC34. The total gain of this combination is either 0.33 or 3.3 depending on the setting of S5D. Trimmer R180 provides calibration for the distortion measurement.

Provision is also made to monitor the input level with the meter circuits. This makes it possible to make a complete THD measurement on a piece of equipment without any other test instruments. Selection of distortion or level as the quantity to be measured is accomplished by S6. In the "Level" position, an attenuated output from the bandpass filter is applied to the meter circuits. The full-scale "Level" range then corresponds to the setting of the input attenuator. Note that this provides a narrowband measurement of the input signal level.

The distortion product signal is then applied to the meter circuit, consisting of IC36 and IC37. IC36 is connected as a unity-gain inverting feedback amplifier which has two feedback paths, one for positive output-signal excursions (D23) and one for negative output excursions (D22). Positive and negative half-wave rectified signals thus appear at the two feedback resistors. The negative half-wave rectified signal and half the unrectified input signal are added at the input of IC37 to produce a full-wave rectified result. This amplifier also provides appro-

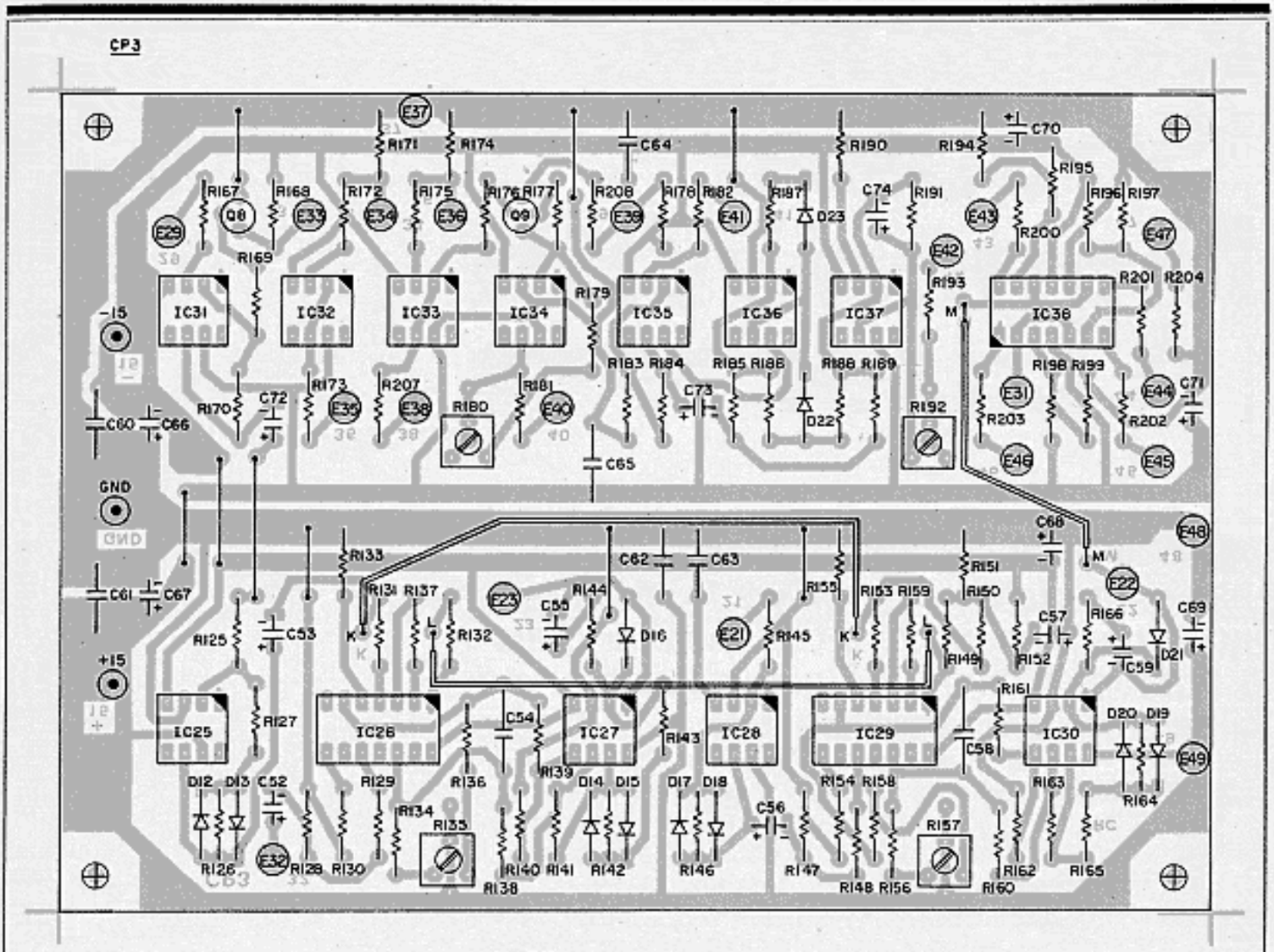

Fig. 24 — Component placement for CP3.

priate low-pass filtering of the result. The single-ended output of IC37 is then used to drive the meter movement.

The status indicator circuits indicate whether the incoming level is too high or too low for proper analyzer operation, and whether the incoming frequency is too high or too low for the auto tune circuits. A quad op-amp comparator (IC38) drives the four indicator LEDs.

The frequency indicator circuit monitors the gate voltage on the frequency control FET (Q5) to see if the frequency is within the tuning range. If the gate voltage is zero or positive, the frequency is too low, and the "Low" LED is lit. If the voltage is more negative than -12 V, the FET is pinched off and the frequency is too high.

The input level indicator circuit monitors the a.g.c. control voltage in the auto-set level circuit. If this voltage goes more negative than -3.5 V, indicating that the input level is more than 11.5 dB above the nominal 1-V internal operating level, the "High" LED will be lit. Similarly, a level more than 11.5 dB below the nominal operating level will light the "Low" LED.

Power Supply

The regulated ±15 V power supply for the analyzer is shown in Fig. 20. The circuit employs a full-wave bridge rectifier and standard three-terminal regulator ICs.

The input circuit, bandpass filter, product amplifiers and auto-set level circuits are realized on printed circuit board CP2. Its layout is shown in Fig. 21 and the component placement diagram is shown in Fig. 22. The auto tune control, product filter, meter and status indicator circuits are realized on CP3. Its layout is shown in Fig. 23, while component placement is illustrated in Fig. 24.

This completes the description of all of the circuitry in the THD analyzer. Next month we'll conclude with construction details, the adjustment procedure, troubleshooting, and performance data.