BUILD A HIGH PERFORMANCE THD ANALYZER

PART ONE

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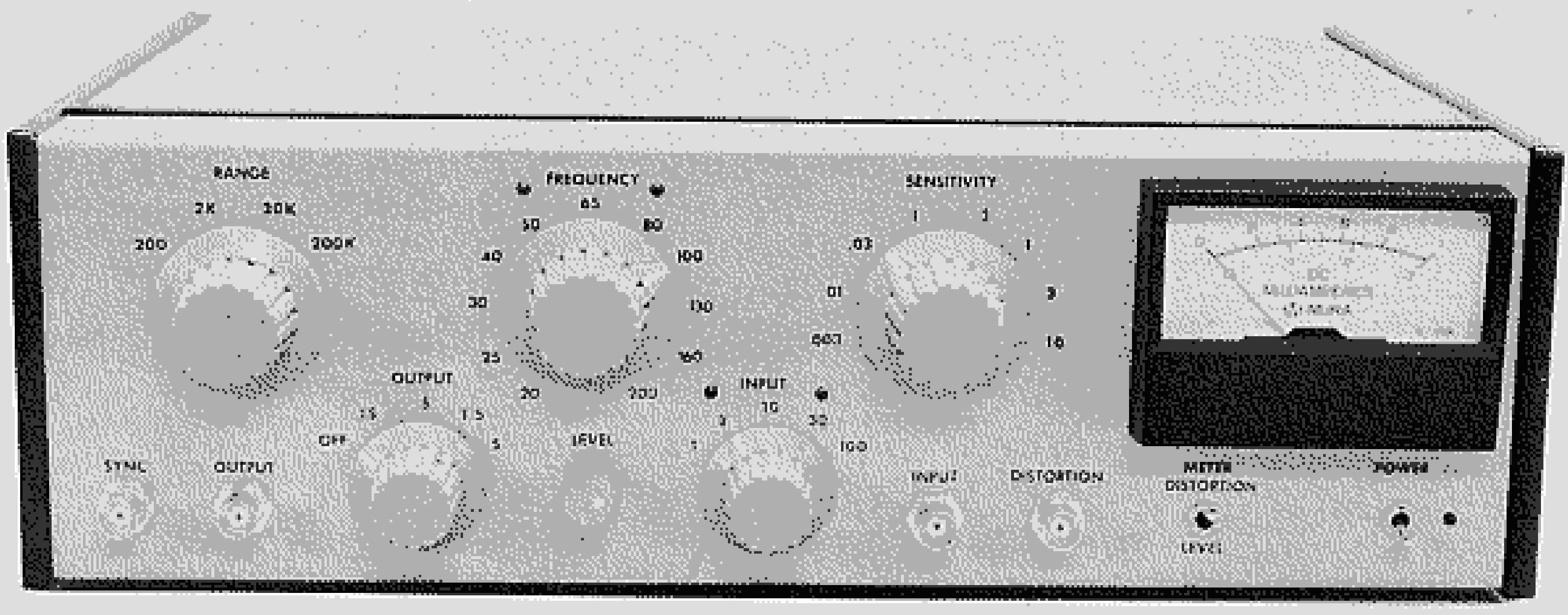

The Total Harmonic Distortion (THD) analyzer is probably the most widely used instrument for evaluation of distortion in audio systems. Unfortunately, those analyzers which are good enough to evaluate contemporary equipment generally cost in the neighborhood of $2,000. Because of a careful selection of features and a topology which lends itself to realization with low-cost components, the analyzer described in this article can be constructed for a fraction of that cost, while providing a measurement floor on the order of 0.001 percent across the full audio band.

A typical measurement setup of a THD analyzer is shown in Fig. 1. It consists of a low-distortion oscillator feeding the Unit Under Test (UUT) which in turn feeds the THD analyzer; an oscilloscope is optionally used to observe the waveform of the distortion products. (In most high-performance THD analyzers, the oscilloscope and analyzer are in one unit.) It is well known that a nonlinearity in the UUT, when adequately excited by a sine wave (the so-called "fundamental"), will produce at the output harmonics of the sine wave in addition to the fundamental. The principle of the THD analyzer is to remove the fundamental entirely and measure what is left. This removal of the fundamental is usually achieved with an extremely sharp and deep notch filter centered on the fundamental frequency.

The 'scope photo in Fig. 2 shows the fundamental sine wave in the top trace and a typical distortion waveform in the bottom trace. Viewing the distortion in the "time domain" is very useful in evaluating the nature of the distortion mechanism. Here, the disturbances near the zero crossings of the fundamental imply that crossover distortion exists. As far as audibility is concerned, for a given magnitude of distortion, smooth or "soft" distortion waveforms are preferable to jagged or "harsh" waveforms.

How THD Analyzers Work

We can get a feel for some of the analyzer requirements by seeing what the desired performance specification implies. Here, our goal is a measurement floor of less than 0.001 percent. This means that if we bypass the UUT, that which remains after the fundamental is rejected is less than 0.001 percent, or 100 dB down. The residual will consist of distortion, unrejected fundamental, noise and hum. Clearly, we need a very good oscillator, one with distortion at least 10 dB down from the floor, or better than 0.0003 percent. In addition, low-noise, low-distortion electronics throughout the analyzer are mandatory.

Similarly, the notch filter should probably have at least 110 dB of rejection, while attenuating the closest harmonic (the second) by less than, say, 0.5 dB. Such a sharp notch is normally difficult to achieve and even more difficult to tune manually. This problem is dealt with in most high-performance analyzers by automatic tuning circuits, often termed "auto tune" [1]. Notch filters are generally realized by passing the signal through two paths with differing phase and/or amplitude characteristics so that the two resulting outputs are equal and of opposite phase only at the center frequency. When combined, the signals thus cancel each other at the center frequency. It can be seen that an automatic tuning system must exert two types of control: One to assure the proper phase relationship at the notch frequency, and one to assure that the amplitudes of the two signals are exactly equal at the notch frequency so that full cancellation can occur. As we shall see later, these two control circuits each function by examining different characteristics of the output of the notch filter and then adjusting notch filter control elements accordingly. The auto-tune circuits of a THD analyzer are generally responsible for a substantial portion of the overall cost, but they are virtually indispensable. With well-designed auto-tune circuits, rejection of the fundamental is so complete that analyzer internal distortion and noise generally dominate the residual and establish the measurement floor.

To make maximum use of the convenience associated with auto tune, it is best to have the oscillator packaged in the analyzer so that its frequency can be controlled in step with that of the analyzer. This also tends to reduce the control range required of the auto-tune circuits, making them less prone to limit analyzer performance.

An additional feature found in most better analyzers is called "auto set level." In analyzers without this feature, a level-setting calibration adjustment must be made whenever the input level is changed. An auto set level feature permits the input level to the analyzer to change over some range, say ±10 dB, without affecting the calibration of the distortion meter. It is achieved with a type of a.g.c. circuit which adjusts the gain in the measurement path (after the notch filter) downward in direct proportion to increases in input level.

Finally, many analyzers include high-pass and low-pass filters of varying complexity and flexibility to optimize performance. These distortion product filters are placed in the measurement path after the notch filter. Generally, a high-pass filter is used to minimize the effect of hum in the UUT on the measurement. Low-pass filters are usually employed to limit the measurement bandwidth (to minimize noise) while passing all of the harmonics of interest (e.g., up to the tenth).

Practical Analyzer Design

My goal here was to provide a THD analyzer design capable of state-of-the-art performance which can be constructed at moderate cost and with readily available parts. At the same time, I felt that retaining the features of a built-in oscillator, auto tune, auto set level, and product filtering was essential. One compromise made to keep down costs was to limit the number of switch-selectable operating frequencies to 10 evenly spaced frequencies per decade from 20 Hz to 200 kHz. Another cost saving resulted from the extensive use of ICs, even in the most critical circuits. In particular, the superb distortion performance of the 5534 operational amplifier made this possible.

A major expense in many analyzers is due or related to the control elements in the auto-tune circuits. The use of so-called "state-variable filters" in both the oscillator and the notch filter in this analyzer permitted the use of inexpensive FETs as the control elements in these circuits. The greater immunity to control-element nonlinearities of these filters has been pointed out in [2]. The topology of these filters also permits the use of ±10 percent capacitors where precision components would normally be required. While several sets of four identical range-selection resistors must be matched to within ±1 percent, the absolute value of these resistors is not critical. Thus, a patient constructor with a digital VOM or simple resistor bridge can select matched sets from standard 5 percent carbon-film resistors. It's highly unlikely that you won't find four or more resistors matched to within ±1 percent among a group of ten ±5 percent carbon-film resistors purchased at the same time.

The exterior and interior views of the completed analyzer are shown in Figs. 3 and 4. The circuitry of the analyzer resides on one small and two medium-sized single-sided printed circuit boards; the regulated power supply is housed in a small metal box at the rear. As can be seen from the photo in Fig. 4, the major part of the construction effort is in the range and frequency switch wiring. As a guide to cost, the three circuit boards and their associated components will typically cost about $160. The cabinet, power supply, meter, switches, switch-mounted components, etc. will represent additional expenses.

Before proceeding, one word of caution is in order. *This ambitious and moderately expensive project should not be attempted by anyone who has not previously built and troubleshot electronic construction projects. Anyone who does not own or have access to an oscilloscope should also think twice before embarking on it.* This is a challenging construction project requiring considerable effort and patience, but the payoff is great for anyone who wants a THD analyzer with state-of-the-art performance.

Fig. 1 — Typical measurement setup of a THD analyzer.

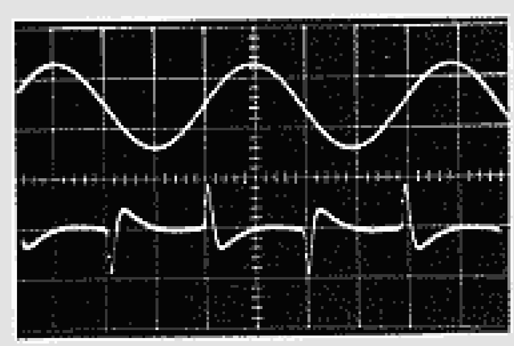

Fig. 2 — 'Scope photo showing the fundamental sine wave (top trace) and a typical crossover distortion waveform (bottom trace).

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Fig. 3 — Exterior view of the completed THD analyzer.

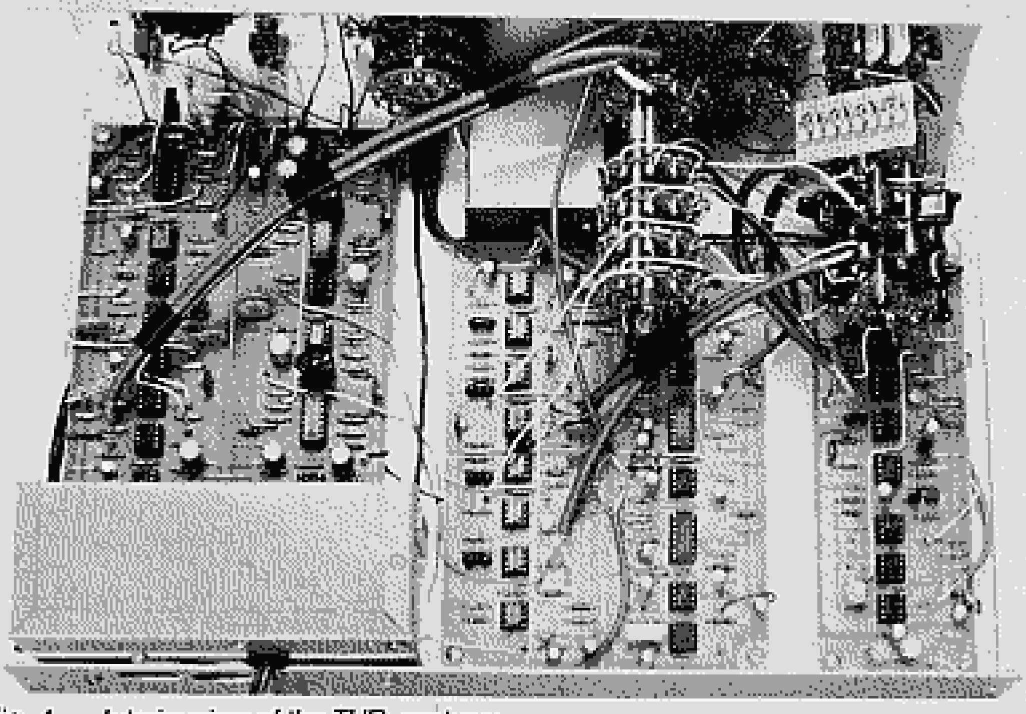

Fig. 4 — Interior view of the THD analyzer.

Overall Design

A block diagram of the complete analyzer is shown in Fig. 5. We'll now proceed with a brief overview of the analyzer's operation at the block diagram level before moving on to more detailed descriptions of the individual circuits.

The signal source resides on a single p.c. card, CP1, and consists of a state-variable oscillator, the necessary amplitude stabilizing circuits, an output amplifier, a level control, and an output attenuator. The amplitude control circuit is essentially a level detector which generates a d.c. error signal to feed the amplitude control multiplier. The latter controls the amount of positive feedback in the oscillator and consists of an FET and an operational amplifier.

The input circuits, controllable notch filter, auto-set level circuit, and distortion product amplifiers are located on a second p.c. card, CP2. The notch filter consists of a differential amplifier which is fed the input signal and a version of this signal which has passed through a state-variable bandpass filter whose frequency and gain are controlled electronically. At the center (fundamental) frequency, both inputs to the differential amplifier are identical in phase and amplitude, leaving only the distortion products at its output. The bandpass filter is sufficiently narrow that its output is very small at the second harmonic and higher frequencies, resulting in less than 0.5 dB of attenuation at the second harmonic. Operation of the notch filter is illustrated by the frequency response curves in Fig. 6.

The auto-set level circuit consists of two voltage-controlled amplifiers (VCAs) to which are fed identical control signals so that their gains vary in the same fashion. One VCA is in the path of the distortion product signal, while the other ("reference" VCA) is fed the output (the filtered fundamental) from the state-variable bandpass filter. The latter VCA feeds a level detector whose d.c. output controls both VCAs. The a.g.c. loop formed by the level detector forces the output of the reference VCA to be at a fixed reference level. Thus, if the input signal level doubles, the gain of both VCAs will be halved, resulting in the proper gain correction being applied to the distortion product path. Both VCAs are realized from inexpensive 1496-type balanced modulator ICs and achieve a control range of ±20 dB with better than ±0.5-dB tracking. Notice that the distortion performance of the VCAs need not be exceptionally good because the one in the measurement path is passing only distortion products. Placement of an a.g.c. circuit ahead of the notch filter would necessitate the use of an extremely low-distortion VCA and might also compromise the noise floor of the instrument.

The auto-tune control circuits, product filters, status indicator circuit, and meter amplifier are located on a third p.c. card, CP3. The auto-tune control circuits consist of amplitude and frequency detectors which produce d.c. error signals to control the gain and center frequency of the state variable bandpass filter. These detectors function by looking for small amounts of fundamental in the output of the notch filter.

The principle of operation is as follows: An amplitude error between the two signals at the inputs of the differen-

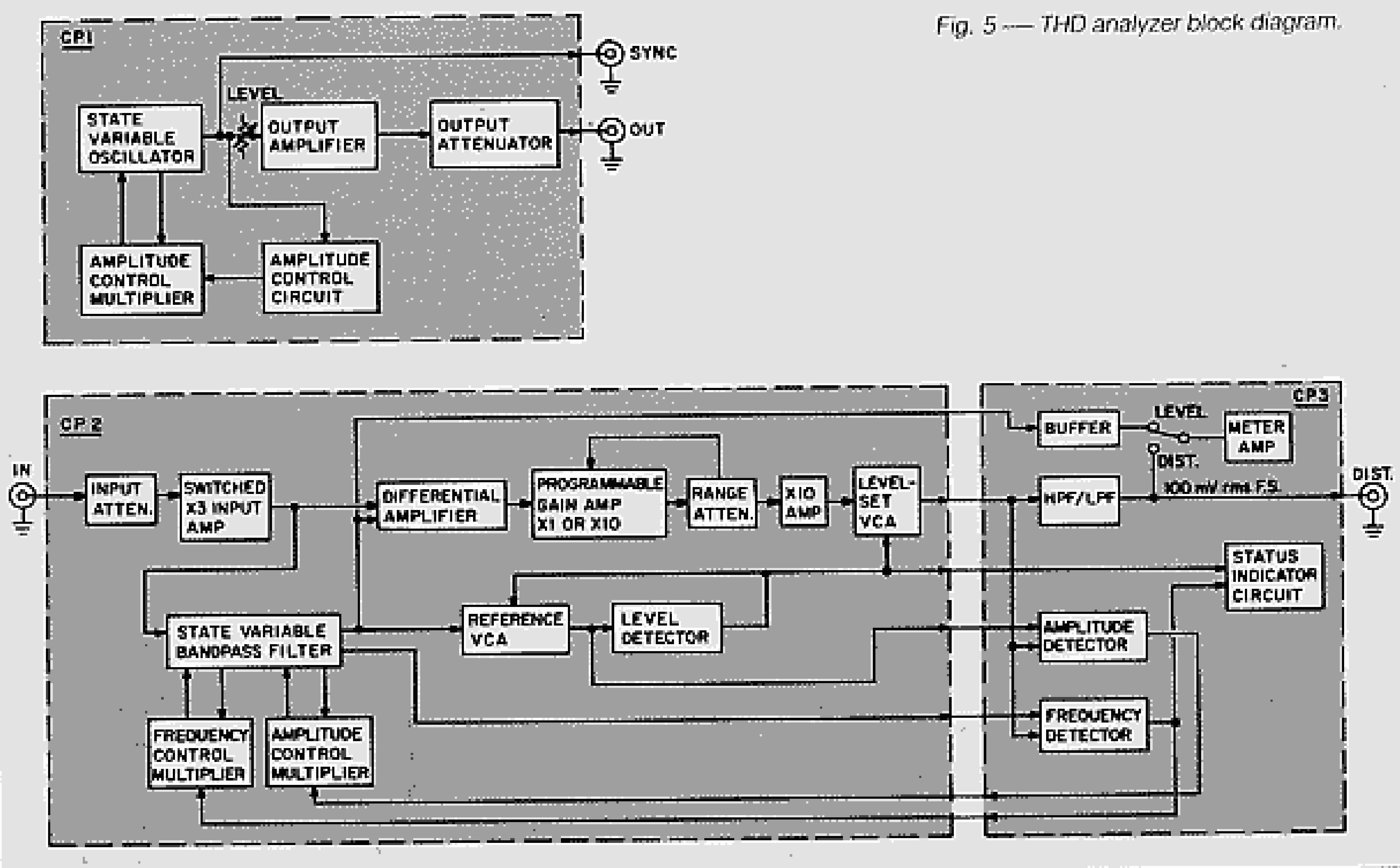

Fig. 5 — THD analyzer block diagram.

tial amplifier will result in a small amount of in-phase (or 180-degree out-of-phase) fundamental at the output of the notch filter. The polarity of this error signal indicates which direction of amplitude adjustment is necessary. Similarly, but less obviously, a frequency error in the bandpass filter will result in a phase error between the two signals at the differential amplifier. This will result in a small amount of fundamental component at the output of the notch filter whose phase is lagging or leading 90 degrees (quadrature) relative to the fundamental. Whether the component is lagging or leading indicates which direction of frequency adjustment is necessary.

Each detector functions by comparing the output of the notch filter (after the auto-set level VCA) to a version of the fundamental supplied by the bandpass filter. The amplitude detector looks for in-phase fundamental components by making its comparison with an in-phase version of the fundamental supplied by the bandpass filter. Similarly, the frequency detector looks for quadrature fundamental components by making its comparison with a 90-degree phase-shifted version of the fundamental, also conveniently supplied by a different output of the bandpass filter. The ready availability of this quadrature fundamental signal is an additional advantage of the state-variable filter.

The d.c. control signals from the level and frequency detectors also feed a status indicator circuit. This circuit drives front panel LEDs which indicate whether the input signal is too high or too low and also whether the input frequency is too high or too low (useful when a source other than the internal oscillator is used).

The high-pass and low-pass product filters in this design are both second-order (12 dB/octave) designs whose cutoff frequencies track changes in the selected fundamental frequency. These tracking filters substantially improve the measurement floor and simplify use of the analyzer by automatically providing optimal filtering regardless of the fundamental frequency setting.

The high-pass filter falls off at 12 dB/octave below the second harmonic frequency. Its roll-off shape is chosen so as to have a minimal effect on distortion product frequency response. The low-pass filter is a second-order Bessel design which is down 3 dB at the tenth harmonic frequency. The excellent phase response characteristic of this design minimizes waveform distortion of the distortion products, preserving the accuracy of the visual display. The analyzer's overall distortion product frequency response is shown in Fig. 7.

While requiring little in the way of electronics, these tracking filters do add substantially to the complexity of the frequency and range switches, and some builders may prefer a simpler and less expensive alternative. Such an approach, providing the fixed filtering at 400 Hz, 30 kHz, and 80 kHz found on many commercial analyzers, is also described later in this article.

As a convenience, notice that with the flip of a switch (S6), the input level can be directly read with the range selected by the analyzer's input attenuator.

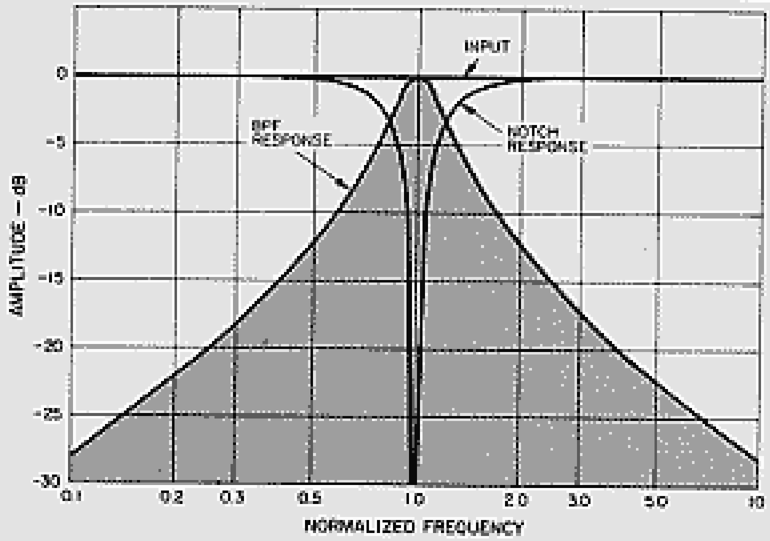

Fig. 6 — Notch filter operation.

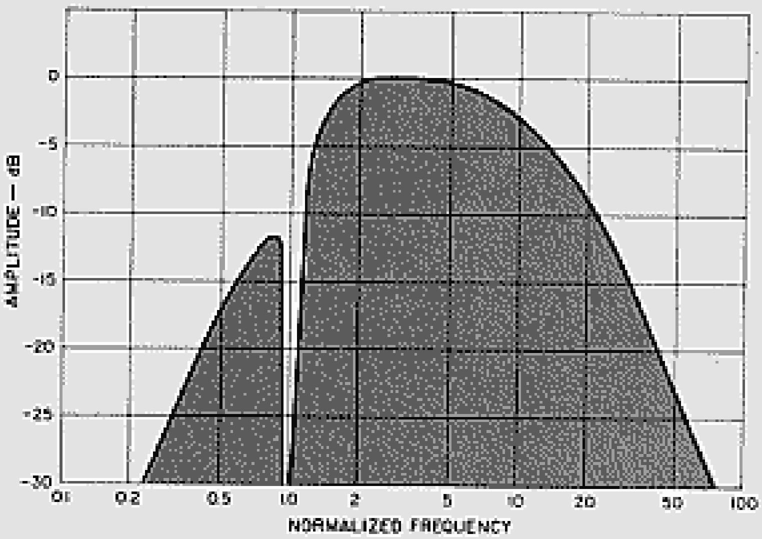

Fig. 7 — THD analyzer frequency response.

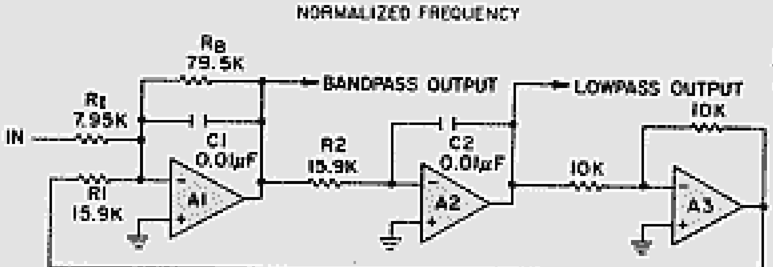

Fig. 8 — A simple state-variable bandpass filter.

State-Variable Filters

Because it is central to the operation of the analyzer, a few words of explanation regarding the state-variable filter are appropriate at this point.

A simple state-variable bandpass filter is shown in Fig. 8. It consists of two integrators and an inverter connected in a loop. An input resistor (R_I) and a second feedback loop (R_B) around the first integrator (A1) complete the filter.

The term "state variable" comes from linear system theory involving solutions to linear differential equations. The state of such a system at a given point in time is completely determined by the values of the system's state variables. The state-variable filter models a second-order differential equation in much the same way as one would model such an equation on an analog computer. In this context, the state variables are the output voltages of the two integrators.

A key to understanding the state-variable filter is the recognition that an integrator has a frequency response which decreases with increasing frequency at 6 dB/octave and introduces a 90-degree lagging phase shift at all frequencies. Let's temporarily ignore the input resistor R_I and the bandwidth-setting resistor R_B and assume that we have a 1-V, 1-kHz signal at the output of A1. Each integrator is formed by a resistor (R1 = R2), a capacitor (C1 = C2), and an operational amplifier. The gain of the integrator is equal to $1/(2\pi RCf)$, where f is the frequency of interest and R and C are the values of R1, R2, C1 and C2. R and C are chosen here for an integrator gain of unity at our 1-kHz operating frequency. The inverter also has a gain of unity. Notice that as the 1-V signal travels around the loop, it picks up 90 degrees from each integrator and 180 degrees from the inverter for a total of 360 degrees, which is the same as zero degrees. Thus, at 1 kHz the signal from A3 feeding the A1 integrator is exactly the signal required to provide and sustain the assumed output. We therefore have an oscillator.

Looking at it from a slightly different view, the feedback from A3 produces a current in R1 which is just equal to the current required by C1 given the assumed signal at the output of A1. The currents into and out of an ideal op-amp's virtual ground (the inverting input when the noninverting input is grounded) must always equal each other.

We can think of an oscillator as a bandpass filter with infinite Q. What if we want finite Q? We add resistor R_B, often called the damping resistor. We now need an input, so R_I is also added. If we make the same assumptions as before, we see that the current in R1 still balances that in C1 at 1 kHz. The current in R_B must therefore come from the input via R_I, so the voltage gain at 1 kHz (the center frequency, f_o) is R_B/R_I, and the phase shift is 180 degrees.

At higher frequencies the current demanded by C1 increases and that provided by R1 decreases. The input must now supply the extra current for C1 as well as that demanded by R_B. A larger input is thus required for a given output, corresponding to decreased gain. By a similar argument, the gain can be seen to decrease at frequencies below f_o as well. We thus have a bandpass characteristic. The Q of this filter is proportional to the value of R_B. The center frequency, f_o, will always be the frequency at which the gain around the main loop is unity. This means that the center frequency can be conveniently changed by altering R, C, the inverter gain, or any combination of these.

With a bit more reasoning, it is easy to demonstrate that the output of the second integrator (A2) provides a 12 dB/

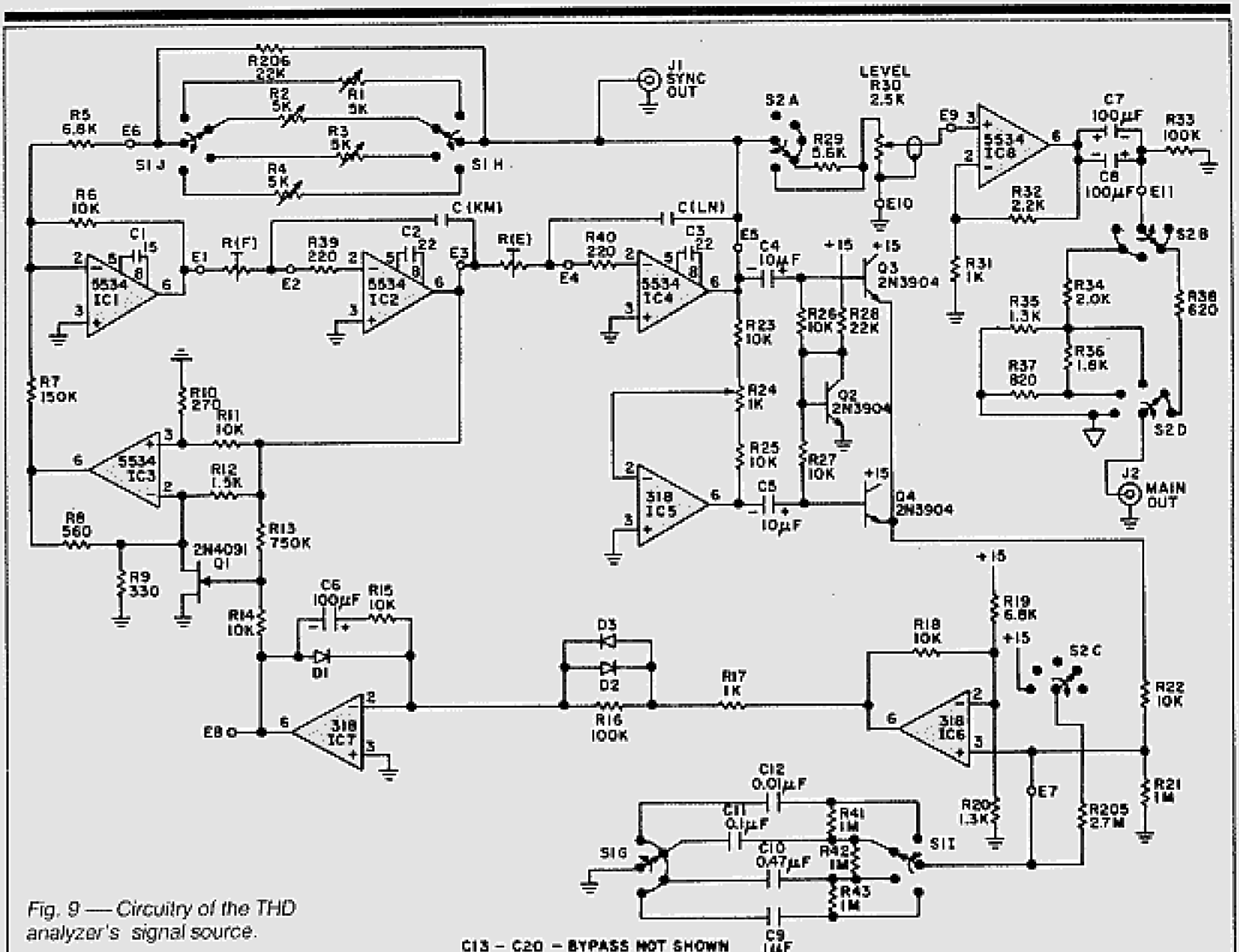

Fig. 9 — Circuitry of the THD analyzer's signal source.

octave low-pass characteristic. Notice that the phase of this output lags that of the bandpass output by 90 degrees at all frequencies. This feature is used to provide the required 90-degree phase-shifted fundamental signal to the frequency detector in the auto-tune circuit.

The Signal Source

With a solid understanding of the state-variable filter, operation of the state-variable oscillator is quite simple. As in the earlier example, we remove R_I and R_B as a start.

As with any linear oscillator, we must provide a means to control the amplitude of the oscillations, i.e., provide a type of a.g.c. circuit. Recognizing that the presence of R_B produced negative feedback around the first integrator which tended to damp out oscillations, we can reason that a feedback circuit around A1 which can provide variable amounts of negative or positive feedback will allow us to control the oscillations. Negative feedback will cause the oscillations to decay, while positive feedback will cause them to grow. This can be accomplished with a multiplier and a resistor in place of R_B. To complete the oscillator, we must add a control circuit to measure the amplitude of the oscillations, then compare it to a fixed reference, and finally deliver a d.c. error signal to the control input of the multiplier.

The complete schematic of the signal source is shown in Fig. 9. First, a word about notation and conventions used on the schematics in this article. For simplicity, power-supply bypass capacitors and power-supply connections to standard pin-out operational amplifiers (+15 V to pin 7, -15 V to pin 4) are not shown. Off-board interconnection terminals are designated with an "E" number. Terminals on different boards which are connected together have the same E designation.

Each pole of a multi-pole rotary switch is designated with a letter, beginning with "A" closest to the front panel. Wafers with two poles have the left-hand pole (as viewed from the front panel) designated with the earlier letter in the alphabet; the letter for the right-hand pole is next in the alphabet. Arrows on switch wipers indicate clockwise rotation as seen from the front panel. Tuning resistors are designated by the letter of the switch pole on which they are mounted (each resistor is mounted between adjacent switch positions on a given pole). Tuning capacitors are mounted between two adjacent wafers on the range switch, and they are designated by the letters corresponding to the two switch poles to which they connect.

Because of the large amount of wideband gain packaged in this unit, specific approaches have been taken in terms of grounding and shielding strategy to avoid oscillations and interference pickup. Much of this is shown on the schematics to permit easy duplication. The symbol, one of three different grounding symbols on the schematics, denotes a single-point chassis ground located at the input jack. All leads with this symbol are connected directly to this single point. The symbol denotes a secondary single-point signal ground on CP2 (Figs. 12 and 13, Part II). This ground is connected to the single-point chassis ground via the shield of the input lead to CP2. The symbol denotes ordinary multi-point circuit grounding. Each circuit board has its ordinary circuit ground connected to the single-point chassis ground, and positive and negative supply voltage is also distributed on a single-point basis from the location of the single-point chassis ground.

Returning to the circuit discussion, the oscillator proper in Fig. 9 consists of IC1 (inverter), IC2 and IC4 (integrators). Frequency-setting resistors R(F) and R(E) are mounted on frequency switch S3, while the corresponding capacitors C(KM) and C(LN) are mounted on range switch S1. Notice that the circuit has been slightly rearranged from that of Fig. 8, with the inverter "up front" and with the amplitude control feedback (IC3) encompassing both the inverter and the integrator. This arrangement permits frequency changes to be made by changing the switch-selected resistors without altering other operating characteristics of the oscillator. The analog multiplier for amplitude control is realized by op-amp IC3 and FET Q1. Notice also that each range has its own frequency trimmer (R1 to R4) to allow close matching of the oscillator frequency to that of the analyzer notch filter without requiring precision frequency-setting capacitors.

The output of the oscillator is taken from IC4, which would correspond to the low-pass output of the filter in Fig. 8. This provides lower distortion and points to a significant advantage of the state-variable approach [2.] Given low-distortion amplifiers, the dominant distortion in an audio oscillator results from nonlinearity in the amplitude control element (here the multiplier) and ripple in the "d.c." control signal as a result of the detection process in the amplitude control circuit. In either case, this distortion is injected at the inverter (IC1) in this design. The two integrators between this point and the output provide a 12 dB/octave roll-off to these injected harmonics, thus affording a 4-to-1 reduction ratio in second harmonic and a 9-to-1 reduction in the more significant third harmonic. The integrators also tend to filter out noise, permitting the amplitude control multiplier to operate at a lower signal level, thus reducing its distortion from the start. These same advantages are also used in the analyzer notch filter.

As mentioned above, the amplitude control circuitry can be a major source of distortion in an audio oscillator. It is therefore important that ripple in the control signal be minimized by providing adequate filtering. However, it must also be realized that what we are dealing with here is a feedback control system, and stability must be considered. Because heavy filtering of the control signal introduces delay in the feedback loop which will decrease stability, we have conflicting requirements. A further strain on stability is generated by the need to have very high d.c. gain in the control circuit to minimize output amplitude errors and thus provide a very flat frequency response. The control circuit used in this design deals with these problems.

The detector portion of the amplitude control circuit includes IC5 and Q2 to Q4. Balanced oscillator output signals are provided by IC4 and inverter IC5 to the full-wave rectifier composed of transistors Q3 and Q4. Transistor Q2 provides a forward bias equal to one base-emitter drop to Q3 and Q4 so as to minimize detection errors resulting from their turn-on voltage requirement. The use of a full-wave rectifier greatly reduces the magnitude of the ripple in the control signal. The trimmer potentiometer in the feedback path of IC5 permits adjustment for perfect balance of the two signals feeding Q3 and Q4. This minimizes distortion by minimizing ripple.

The rectified signal is filtered by the capacitor connected to E7 whose value is selected by the range switch (S1) to optimize the control dynamics for each frequency range. The filtered d.c. is then applied to differential amplifier IC6 where it is compared to a supply-derived d.c. reference voltage to produce an error voltage. The control circuit establishes the desired operating level of about 1.6 V rms at IC4's output.

From IC6 the error signal proceeds to FET driver amplifier IC7 through a nonlinear network. Under quiescent conditions the error voltage is small, and the gain in this path is relatively low so that ripple transmitted to the FET gate will be minimized. Under large-error conditions, such as just after a range change, the gain in this path becomes large to speed up amplitude stabilization. This is accomplished by diodes D2 and D3, which bypass R16 under these conditions.

For a.c. error signal components, IC7 operates as a simple inverting stage whose gain is set by R15. This assures stability of the feedback loop formed by the a.g.c. circuit. However, for d.c. error signals capacitor C6 provides for an extremely large gain in IC7. In essence, IC7 looks like an integrator at low frequencies. The output from this integrator will continue to change and adjust the gate voltage of Q1 until the error voltage from IC6 goes to zero. Following a range change, it takes the integrator about five seconds to drive the oscillator amplitude to within 0.1 dB of its final value. Diode D1 prevents a large forward bias from ever being applied to Q1.

The amplitude control multiplier is implemented by IC3 and FET Q1. The FET acts as a variable resistance, with the resistance controlled by the d.c. voltage applied to its gate by IC7. As the gate voltage varies from zero to a negative value equal to its "pinch-off" voltage (typically 5 to 10 V), its resistance from drain to source varies from about 25 ohms to infinity. IC3 is connected as a differential amplifier whose positive and negative inputs each receive a portion of the signal applied by IC2. Such a circuit can provide inverting or noninverting gain depending upon the relative balance between the circuits associated with the inverting and noninverting inputs of the op-amp. FET Q1 controls this balance. When the FET resistance is low, the noninverting gain exceeds the inverting gain so that a noninverting overall characteristic results. When the FET resistance is high, the opposite action results. At some intermediate FET resistance, the circuit is balanced and the gain is zero.

FETs are not perfectly linear resistors; their drain-to-source resistance tends to be a function of the drain-to-source voltage. Such a nonlinearity can create distortion, making this a major concern. One way of minimizing this distortion is to operate the FET at the lowest possible signal level across it that is consistent with acceptable noise performance. The excellent low-noise performance of the associated 5534 op-amp makes it possible here to operate at a level of only about 40 mV rms across Q1. This is established by the voltage divider which applies a fixed level of about 40 mV rms to the noninverting input of IC3. Because of the virtual short existing between the input terminals of an op-amp operating with negative feedback, this voltage also must appear at the inverting terminal of IC3, and thus across Q1.

A second way of reducing FET distortion involves a well-known technique wherein half of the drain-to-source signal is fed back to the gate of the FET. This provides a first-order correction for the nonlinearity, practically eliminating second harmonic distortion and leaving only a small amount of third and higher order harmonic distortion. This feedback is provided by the 750-kilohm resistor (R13) connected to the gate.

The remainder of the signal source consists of the level control (R30), the output amplifier (IC8), and the output attenuator. The level control provides continuous adjustment of the output amplitude, while the output attenuator provides maximum output ranges of 5 V, 1.5 V, 500 mV, and 150 mV. An off position is also provided which effectively kills oscillations, and it should be used when a different signal source is being employed so that crosstalk from the oscillator into the analyzer cannot affect results. The attenuator establishes a constant output impedance of 600 ohms. A fixed 1.6-V rms "sync" output is also provided by the signal source, which is useful as the trigger source for an oscilloscope used to visually monitor the distortion signal output of the analyzer.

Having discussed the overall analyzer in general and the signal source portion in detail, we now conclude Part I. Next month, in Part II, I will describe the remaining circuits in detail. Construction details and adjustment procedures will be covered in Part III.

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